In re LENOSKI ET AL., Application No. 09/519,282
Amendment D

Amendments to the Claims:

The listing of clams will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

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Claim 1 (previously presented): A method performed by a packet switch, the packet switch including one or more multistage interconnection networks, each of said one or more multistage interconnection networks including a plurality of switching stages which include a first switching stage, a final switching stage, and one or more intermediate switching stages in between the first and final switching stages, said or more intermediate switching stages including a broadcast component, the method comprising:

recognizing an error within the packet switch by one of the plurality of switching stages;

sending a particular packet from said one of the plurality of switching stages to the broadcast component through at least a portion of said one or more interconnection networks in response to said recognizing the error, the particular packet including an indication of the error and an indication corresponding to the broadcast component; ~~and~~

notifying a plurality of input components of the packet switch of the error, said notifying including sending one or more packets indicating the error from the broadcast component through at least a second portion of said one or more interconnection networks, said second portion including the final switching stage;

each of the plurality of input components updating one or more status data structures in response to receiving a notification of the error; and

each of the plurality of input components determining which particular path of a plurality of paths leading to a destination output component over which to send a packet received at said respective input component, with the path being determined by referencing said one or more status data structures; which includes ANDing a bit vector representing a set of possible paths leading to the destination output component with one or more bit vectors representing the status the set of possible paths maintained in said one or more data structures to identify a set of available paths, and selecting said particular path from the set of available paths.

Claims 2-8 (canceled)

Claim 9 (currently amended): The method of ~~claim 6~~ claim 1, wherein the one or more data structures include an output availability table to indicate whether a possible path through the packet switching system from the input component to a particular destination is available.

Claim 10 (currently amended): The method of claim 1, further comprising disabling at least one of the plurality of input components from sending packets to a particular destination of the packet switching system when a number of possible paths through the packet switching system leading to ~~a~~ the particular destination falls below a predetermined threshold value as identified by one or more received packets containing indications of one or more errors.

Claims 11-26 (canceled)

Claim 27 (previously presented): The method of claim 10, wherein the predetermined threshold value is greater than one.

Claim 28 (currently amended): The method of claim 1, further comprising disabling at least one of the plurality of input components from sending packets to a particular destination of the packet switching system when a number of possible paths through the packet switching system leading to ~~a~~ the particular destination equals one.

Claim 29 (new): A packet switch including one or more multistage interconnection networks, each of said one or more multistage interconnection networks including a plurality of switching stages which include a first switching stage, a final switching stage, and one or more intermediate switching stages in between the first and final switching stages, said or more intermediate switching stages including a broadcast component, the packet switch comprising:

means for recognizing an error within the packet switch by one of the plurality of switching stages;

means for sending a particular packet from said one of the plurality of switching stages to the broadcast component through at least a portion of said one or more interconnection networks, said means for sending a particular packet being responsive to said means for recognizing the error, and wherein the particular packet includes an indication of the error and an indication corresponding to the broadcast component;

means for notifying a plurality of input components of the packet switch of the error, said notifying including means for sending one or more packets indicating the error from the broadcast component through at least a second portion of said one or more interconnection networks, said second portion including the final switching stage;

means for each of the plurality of input components updating one or more status data structures in response to receiving a notification of the error; and

means for each of the plurality of input components to determine which particular path of a plurality of paths leading to a destination output component over which to send a packet received at said respective input component, with the path being determined by referencing said one or more status data structures; which includes ANDing a bit vector representing a set of possible paths leading to the destination output component with one or more bit vectors representing the status the set of possible paths maintained in said one or more data structures to identify a set of available paths, and selecting said particular path from the set of available paths.

Claim 30 (new): The packet switch of claim 29, wherein said one or more data structures include an output availability table to indicate whether a possible path through the packet switching system from the input component to a particular destination is available.

Claim 31 (new): The packet switch of claim 29, comprising means for disabling at least one of the plurality of input components from sending packets to a particular destination of the packet switching system when a number of possible paths through the packet switching system leading to the particular destination falls below a predetermined threshold value as identified by one or more received packets containing indications of one or more errors.

Claim 32 (previously presented): The packet switch of claim 31, wherein the predetermined threshold value is greater than one.

Claim 33 (previously presented): The packet switch of claim 29, comprising means for disabling at least one of the plurality of input components from sending packets to a particular destination of the packet switching system when a number of possible paths through the packet switching system leading to the particular destination equals one.